

IN THE CLAIMS:

Please amend Claims 1, 5 and 8 as shown below. The claims, as pending in the subject application, read as follows:

1. (Currently Amended) A processor system, which is provided with a built-in processor, a memory controller, an external bus interface that can connect an external processor from outside of a single semiconductor substrate, a processor bus which is connected with the built-in processor and the external bus interface, and a connection unit that mutually connects ~~the built-in processor~~, the memory controller and ~~the external bus interface~~ processor bus on the single semiconductor substrate.

2. (Original) The processor system according to claim 1, wherein the connection unit includes a crossbar switch.

3. (Original) The processor system according to claim 1, wherein the connection unit includes a common bus.

4. (Original) The processor system according to claim 1, further comprising:
a second built-in processor connected to the connection unit on the semiconductor substrate.

5. (Currently Amended) The processor system according to claim 1, further comprising:

enabling means for enabling, in the alternative, either the built-in processor or the external bus interface.

6. (Original) The processor system according to claim 5, wherein the enabling means enables the built-in processor and the external bus interface independently, respectively.

7. (Original) The processor system according to claim 1, wherein the built-in processor and the external bus interface are connected through a bus common to the connection unit.

8. (Currently Amended) The processor system according to claim 1, wherein the built-in processor and the external processor use in common programs stored in a memory controlled by the memory controller.

9. (Original) The processor system according to claim 1, further comprising:

an image data transfer bus connected with the connection unit; and
an image output device interface or an image input device interface connected with the image data transfer bus on the semiconductor substrate.